BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

METHODS OF FORMING SILICON DIOXIDE LAYERS, AND METHODS OF FORMING TRENCH ISOLATION REGIONS

* * * * *

INVENTORS

Sujit Sharan
Gurtej S. Sandhu

ATTORNEY'S DOCKET NO. MI22-826

METHODS OF FORMING SILICON DIOXIDE LAYERS, AND METHODS OF FORMING TRENCH ISOLATION REGIONS

TECHNICAL FIELD

The invention pertains to methods of forming silicon dioxide layers, such as, for example, methods of forming trench isolation regions.

BACKGROUND OF THE INVENTION

Integrated circuitry is typically fabricated on and within semiconductor substrates, such as bulk monocrystalline silicon wafers. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure including, but not limited to, the semiconductive substrates described above.

Electrical components fabricated on substrates, and particularly bulk semiconductor wafers, are isolated from adjacent devices by insulating materials, such as silicon dioxide. One isolation technique uses shallow trench isolation, whereby trenches are cut into a substrate and are subsequently filled with an insulating material, such as, for example, silicon dioxide. In the context of this document, "shallow" shall refer to a distance of no greater than about 1 micron from an

outermost surface of a substrate material within which an isolation region is received.

A prior art method for forming a trench isolation region, such as a shallow trench isolation region, is described with reference to Figs. 1-2. Fig. 1 illustrates a semiconductor wafer fragment 10 at a preliminary step of the prior art processing method. Wafer fragment 10 comprises a substrate 12, a pad oxide layer 14 over substrate 12, and a silicon nitride layer 16 over pad oxide layer 14. Substrate 12 can comprise, for example, a monocrystalline silicon wafer lightly doped with a p-type background dopant. Pad oxide layer 14 can comprise, for example, silicon dioxide.

Openings 22 extend through layers 14 and 16, and into substrate 12. Openings 22 can be formed by, for example, forming a patterned layer of photoresist over layers 14 and 16 to expose regions where openings 22 are to be formed and to cover other regions. The exposed regions can then be removed to form openings 22, and subsequently the photoresist can be stripped from over layers 14 and 16.

A first silicon dioxide layer 24 is formed within openings 22 to a thickness of, for example, about 100 Angstroms. First silicon dioxide layer 22 can be formed by, for example, heating substrate 12 in the presence of oxygen. A second silicon dioxide layer 26 is deposited within the openings by high density plasma deposition. In the context

of this document, a high density plasma is a plasma having a density of greater than or equal to about 10^{10} ions/cm^3.

Fig. 1 is a view of wafer fragment 10 as opening 22 is partially filled with the deposited silicon dioxide, and Fig. 2 is a view of the wafer fragment after the openings have been completely filled. As shown in Fig. 1, the deposited silicon dioxide undesirably forms cusps 28 at top portions of openings 22. Specifically, cusps 28 are formed over corners of silicon nitride layer 16 corresponding to steps in elevation. The cusp formation (also referred to as "bread-loafing") interferes with subsequent deposition of silicon dioxide layer 26 as shown in Fig. 2. Specifically, the subsequently deposited silicon dioxide can fail to completely fill openings 22, resulting in the formation of voids 29, or "keyholes" within the deposited silicon dioxide layer 26.

After providing second silicon dioxide layer 26 within openings 22, the second silicon dioxide layer is planarized, preferably to a level slightly below an upper surface of nitride layer 16, to form silicon dioxide plugs within openings. The silicon dioxide plugs define trench isolation regions within substrate 12. Such trench isolation regions have voids 29 remaining within them. The voids define a space within the trench isolation regions having a different dielectric constant than the remainder of the trench isolation regions, and can undesirably allow current leakage through the trench isolation regions. Accordingly, it is desirable to develop methods of forming trench isolation regions wherein voids 29 are avoided.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming a silicon dioxide layer. A high density plasma is formed proximate a substrate. The plasma comprises silicon dioxide precursors. Silicon dioxide is formed from the precursors and deposited over the substrate at a deposition rate. While the silicon dioxide is being deposited, it is etched with the plasma at an etch rate. A ratio of the deposition rate to the etch rate is at least about 4:1.

In another aspect, the invention encompasses a method of forming a silicon dioxide layer over a substrate wherein a temperature of the substrate is maintained at greater than or equal to about 500° C during the deposition. More specifically, a high density plasma is formed proximate a substrate. Gases are flowed into the plasma, and at least some of the gases form silicon dioxide. The silicon dioxide is deposited over the substrate. While the silicon dioxide is being deposited, a temperature of the substrate is maintained at greater than or equal to about 500° C.

In another aspect, the invention encompasses a method of forming a silicon dioxide layer over a substrate wherein the substrate is not cooled during the deposition. More specifically, a high density plasma is formed proximate a substrate. Gases are flowed into the plasma, and at least some of the gases form silicon dioxide. The silicon dioxide is deposited over the substrate. The substrate is not cooled with a coolant gas while depositing the silicon dioxide.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a fragmentary, diagrammatic, cross-sectional view of a semiconductor wafer fragment at a preliminary step of a prior art fabrication process.

Fig. 2 is a view of the Fig. 1 wafer fragment shown at a prior art processing step subsequent to that of Fig. 1.

Fig. 3 is a diagrammatic, cross-sectional view of a reaction chamber configured for utilization in a method of the present invention.

Fig. 4 is a diagrammatic cross-sectional view of a semiconductor wafer fragment processed in accordance with the present invention. The wafer fragment of Fig. 4 is shown at a processing step similar to the prior art processing step shown in Fig. 1.

Fig. 5 is a view of the Fig. 4 wafer fragment shown at a processing step subsequent to that of Fig. 4.

Fig. 6 is a view of the Fig. 4 wafer fragment shown at a processing step subsequent to that of Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

The present invention encompasses methods of increasing a deposition to etch ratio in a high density plasma reaction chamber during formation of a silicon dioxide layer. A high density plasma reaction chamber 40 is illustrated in Fig. 3. Reaction chamber 40 comprises a vessel 42 surrounded by inductive coils 44. Inductive coils 44 are connected to a first power source 46 which can be configured to provide power, such as, for example, RF energy, within coils 44. Reaction chamber 40 further comprises a chuck 48 configured for holding a semiconductive wafer 45 within vessel 42. Wafer 45 is connected through chuck 48 to a power source 50 which can be configured to, for example, produce RF energy within wafer 45.

In operation, plasma precursor gasses (not shown) are flowed into vessel 42. Power source 46 is utilized to provide a first bias, of, for example, a power of from about 1000 watts to about 8000 watts to inductive coils 44, which generates a plasma 56 within vessel 42. Second power source 50 is utilized to provide a second bias, of, for example, a power of from about 1000 watts to about 5000 watts to wafer 45.

Among the plasma precursor gasses are silicon dioxide precursors such as, for example, SiH_4 and oxygen, as well as other plasma

components, such as, for example, Ar. Plasma 56 can, for example, be formed from a gas consisting essentially of SiH_4, O_2 and Ar. The silicon dioxide precursors form silicon dioxide which is deposited on wafer 45 at a deposition rate. Also, during the depositing, the silicon dioxide is etched at an etch rate.

In prior art processes, the chuck is cooled to maintain the wafer at a temperature of less than or equal to 300° C. In contrast, in a process of the present invention, chuck 48 is not cooled. Accordingly, wafer 10 is permitted to heat within vessel 42 during a present invention deposition process by energy transferred from plasma 56. Preferably, wafer 45 is maintained at temperatures of at least about 500° C, but preferably is removed before its temperature exceeds about 1000° C.

It is observed that a significant etch of the deposited material occurs primarily when wafer 45 is biased within vessel 42. Accordingly, a method for measuring the deposition rate is to remove any bias power from wafer 45, and to keep other reaction parameters appropriate for deposition of silicon dioxide. Silicon dioxide will then be deposited on wafer 45 without etching.

To determine an etch rate occurring within chamber 42 during a deposition process, a wafer 45 having an exposed layer of silicon dioxide is provided within the reaction chamber. The reaction parameters within the chamber are then adjusted as they would be for a deposition process, with the wafer being biased as would occur in a typical

deposition process, but there being no feed of silicon dioxide precursors to the chamber. Accordingly, etching of the silicon dioxide layer occurs without additional growth of silicon dioxide.

Measurements conducted relative to a prior art high density plasma deposition process reveal that a ratio of the deposition rate to the etch rate is less than about 3.4:1 for trenches having an aspect ratio of from about 2.5 to about 1. In contrast measurements conducted relative to a high density plasma deposition process of the present invention reveal that by maintaining wafer 45 at temperatures of at least about 500° C, the ratio of the deposition rate to the etch rate can be increased to at least about 4:1, more preferably to at least about 6:1, and still more preferably to at least about 9:1. The ratio of deposition rate to etch rate varies with an aspect ratio of a trench being filled.

It is observed that the void formation described above with reference to Fig. 1 can be reduced, or even eliminated, by increasing a deposition-to-etch ratio of a high density plasma deposition process.

Referring to Figs. 4-6, a deposition process of the present invention is illustrated. In describing Figs. 4-6, similar numbering to that utilized above in describing the prior art Figs. 1 and 2 will be used, with differences indicated by the suffix "a" or by different numerals. Fig. 4 illustrates a semiconductor wafer fragment 10a shown at a processing step corresponding to that of the prior art wafer fragment 10 of Fig. 1. Wafer fragment 10a can, for example, be a

portion of the wafer 45a illustrated in Fig. 3. Wafer fragment 10a comprises a layer of silicon dioxide 26a deposited over a substrate 12a and within openings 22a. A difference between wafer fragment 10a of Fig. 4, and wafer fragment 10 of Fig. 1, is that the high deposition-to-etch ratio of the present invention has significantly eliminated cusps 28 (Fig. 1). In other words, the high deposition-to-etch ratio of the present invention has achieved a more conformal coating of silicon dioxide layer 26a over the elevational step of an upper corner of nitride layer 16 than could be achieved with prior art processing methods. Such more conformal coating can be referred to as "better step coverage".

Referring to Fig. 5, wafer fragment 10a is illustrated after silicon dioxide deposition has progressed to fill openings 22a with silicon dioxide layer 26a. Wafer fragment 10a of Fig. 5 is illustrated at a processing step analogous to the prior art step illustrated in Fig. 2. A difference between wafer fragment 10a of Fig. 5 and prior art wafer fragment 10 of Fig. 2 is that keyholes 29 are eliminated from fragment 10a.

Referring to Fig. 6, wafer fragment 10a is illustrated after planarizing silicon dioxide layer 26a (Fig. 5) and removing silicon nitride layer 16 to form shallow trench isolation regions 32. Shallow trench isolation regions 32 comprise the planarized second silicon dioxide layer and thermally grown silicon dioxide 24a. Trench isolation regions 32

lack the voids 29 that had been problematic in prior art trench isolation regions.

It is noted that the process of the present invention is described with reference to the reaction chamber construction of Fig. 9 for purposes of illustration only. The present invention can, of course, be utilized with other reaction chamber constructions, such as, for example, transformer coupled plasma reactors.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.